REMARKS

Claims 1 through 3 are currently pending in the application.

This amendment is in response to the Office Action of March 31, 2005.

Double Patenting Rejection Based on U.S. Patent 6,147,316

Claims 1 through 3 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 2 of U.S. Patent 6,147,316. Applicant has responded to this rejection in an amendment filed on June 29, 2005.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on Yabe (U.S. Patent 5,726,074)

Claims 1 through 3 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yabe (U.S. Patent 5,726,074).

Applicant withdraws the remarks in the amendment filed on June 29, 2005, regarding the Yabe reference not being prior art to the claimed inventions.

Applicant asserts that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Turing to the cited prior art, the Yabe reference describes the use of a bar code applied to a wafer to store information regarding the plurality of semiconductor integrated circuits formed on the wafer.

Applicant asserts that the Yabe reference does not and cannot anticipate the claimed inventions of presently amended independent claims 1, 2, and 3 under 35 U.S.C. § 102 because the Yabe reference does not identically describe, either expressly or inherently, each and every element of the claimed inventions in as complete detail as contained in the claims. Applicant asserts that the Yabe reference does not identically describe the element of the claimed inventions of presently amended independent claims 1, 2, and 3 calling for "storing an enhanced reliability testing flag stored in the integrated circuit device associated with a unique

identification code of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires enhanced reliability testing" and "storing a reliability testing flag in the integrated circuit device associated with a unique identification code of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires further reliability testing". In contrast to the claimed inventions of presently amended independent claims 1, 2, and 3 of the present application, the Yabe reference stores information on the wafer using a bar code. Such is not the claimed inventions of presently amended independent claims 1, 2, and 3. Therefore, such claims are allowable.

Applicant submits that claims 1 through 3 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 1 through 3 and the case passed for issue.

Respectfully submitted,

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